Fig. 1

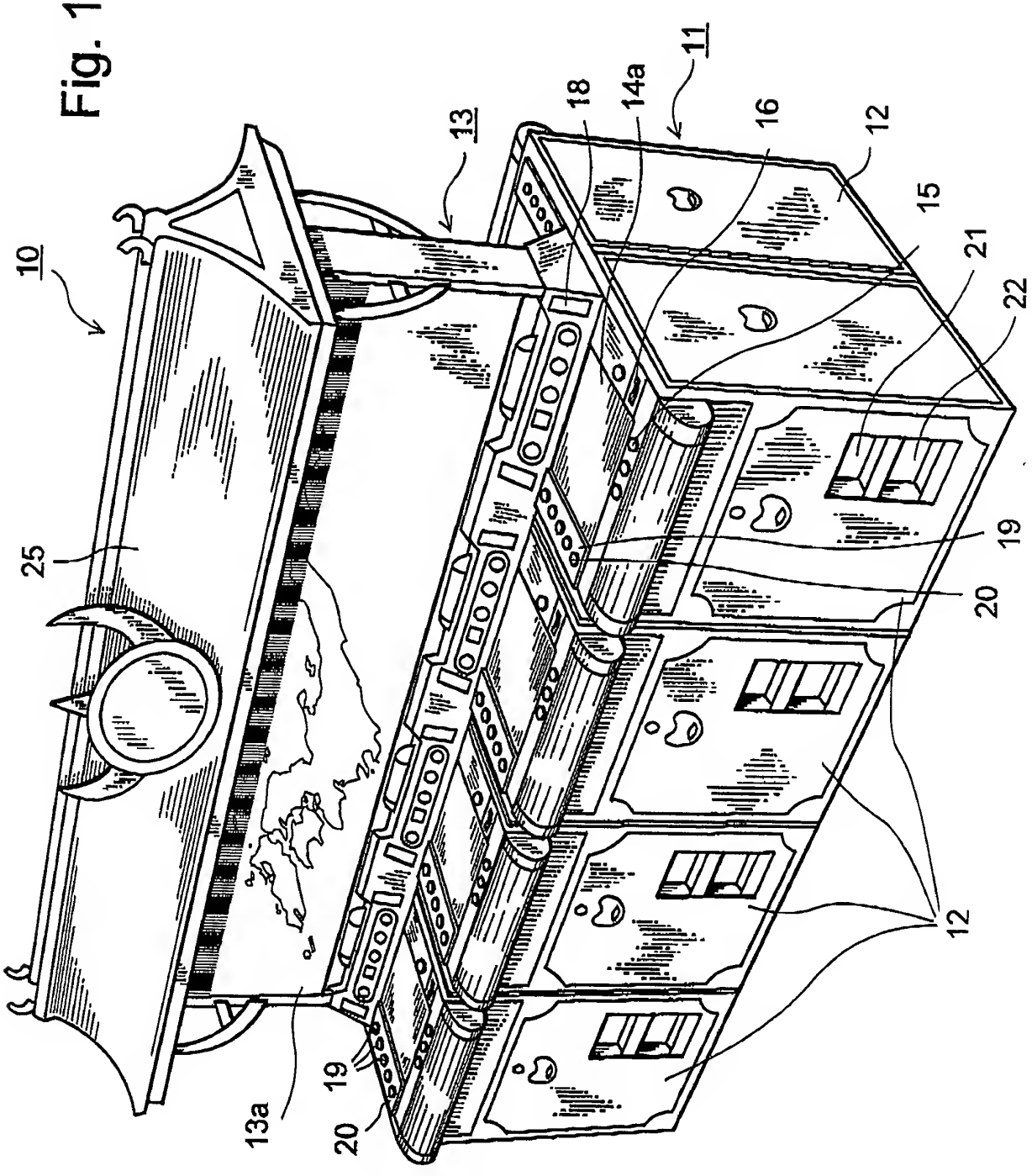


Fig. 2 A

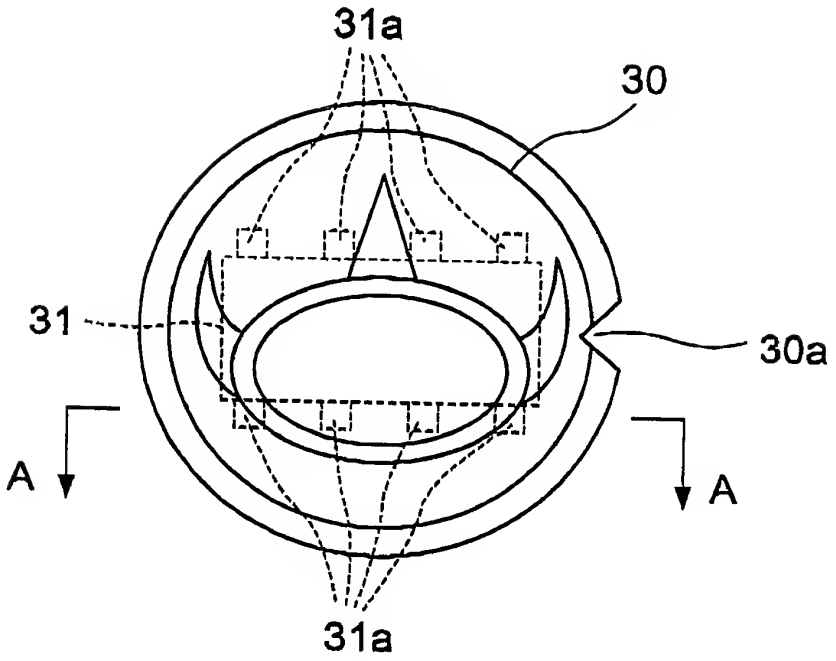


Fig. 2 B

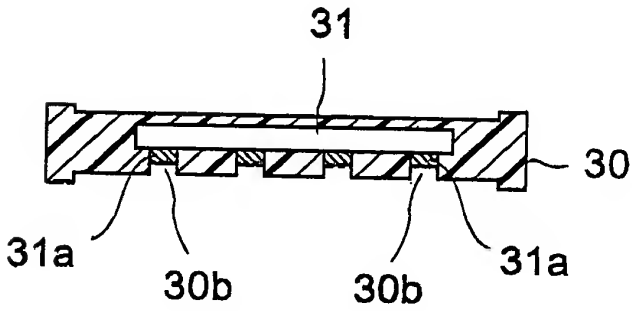


Fig. 3 A

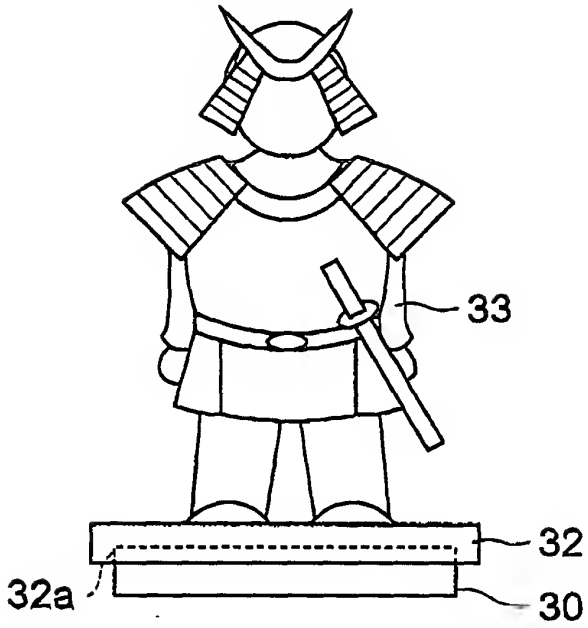


Fig. 3 B

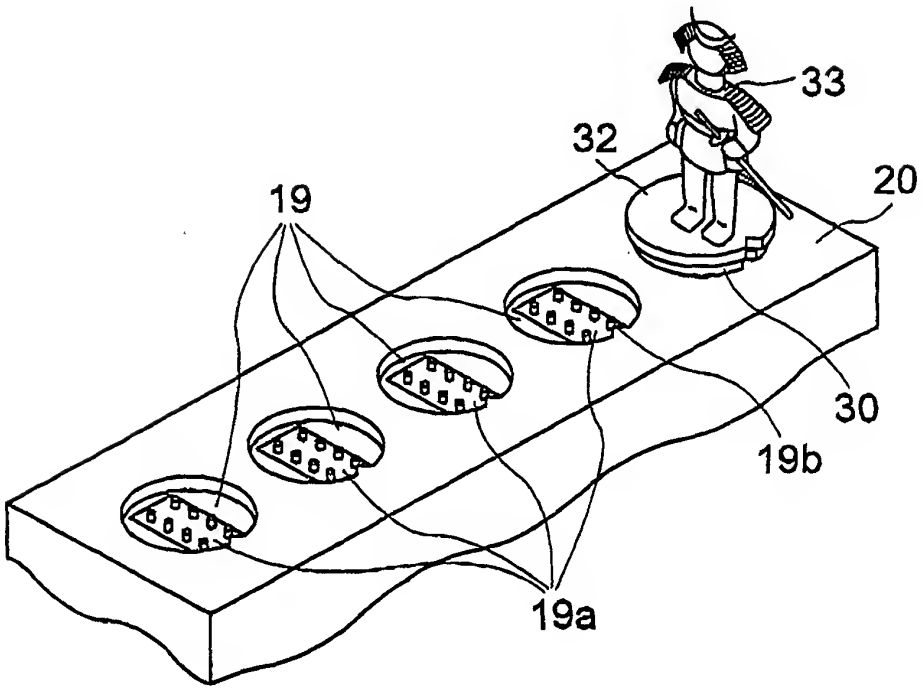


Fig. 4 A

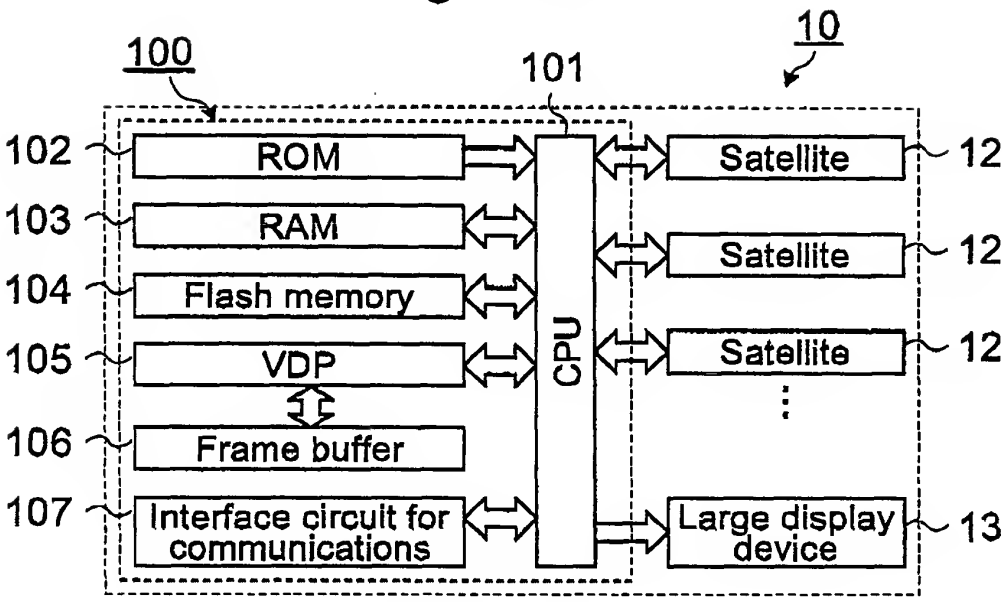

100
101
10
102
ROM
103
RAM
104
Flash memory
105
VDP
106
Frame buffer
107
Interface circuit for communications
CPU
Satellite
12
Satellite
12
Satellite
12
Large display device
13

Fig. 4 B

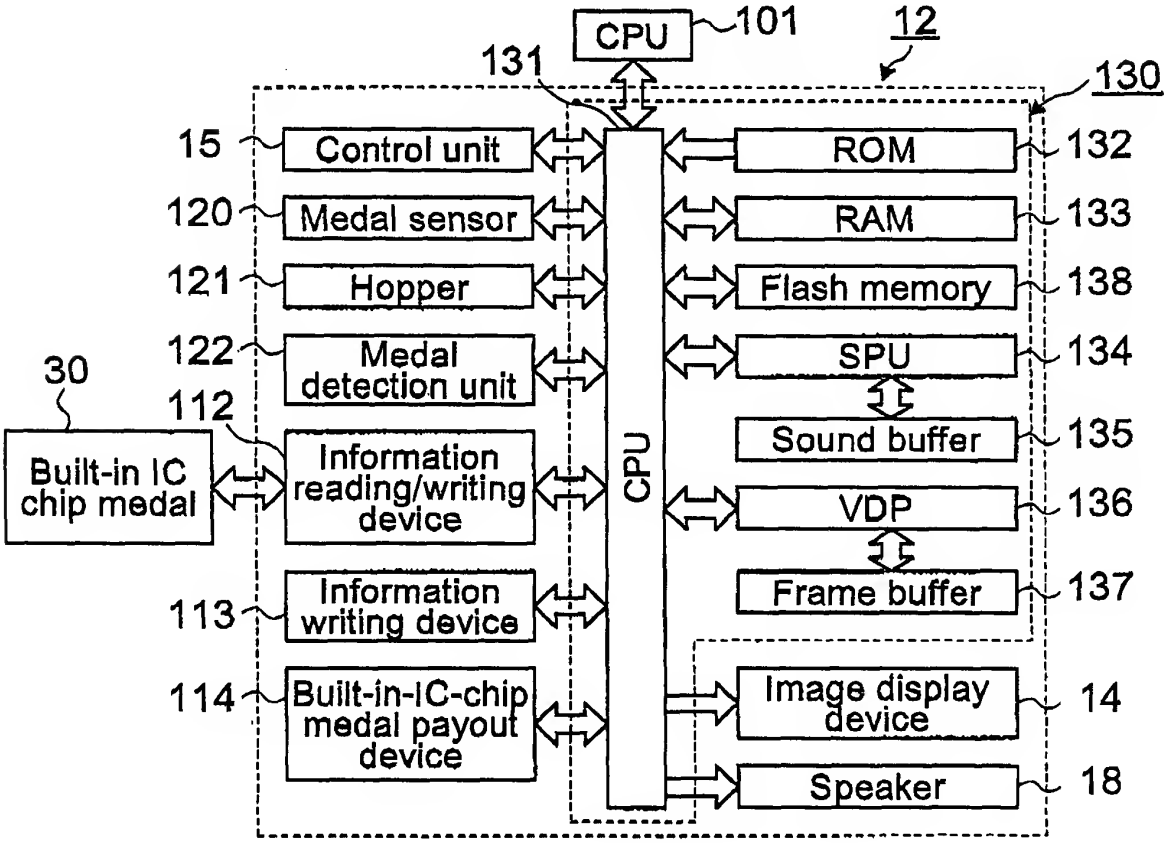

CPU
101
12
131
130
15
Control unit
120
Medal sensor
121
Hopper
122
Medal detection unit
30
112
Built-in IC chip medal
Information reading/writing device
113
Information writing device
114
Built-in-IC-chip medal payout device
CPU
ROM
132
RAM
133
Flash memory
138
SPU
134
Sound buffer
135
VDP
136
Frame buffer
137
Image display device
14
Speaker
18

Fig. 5

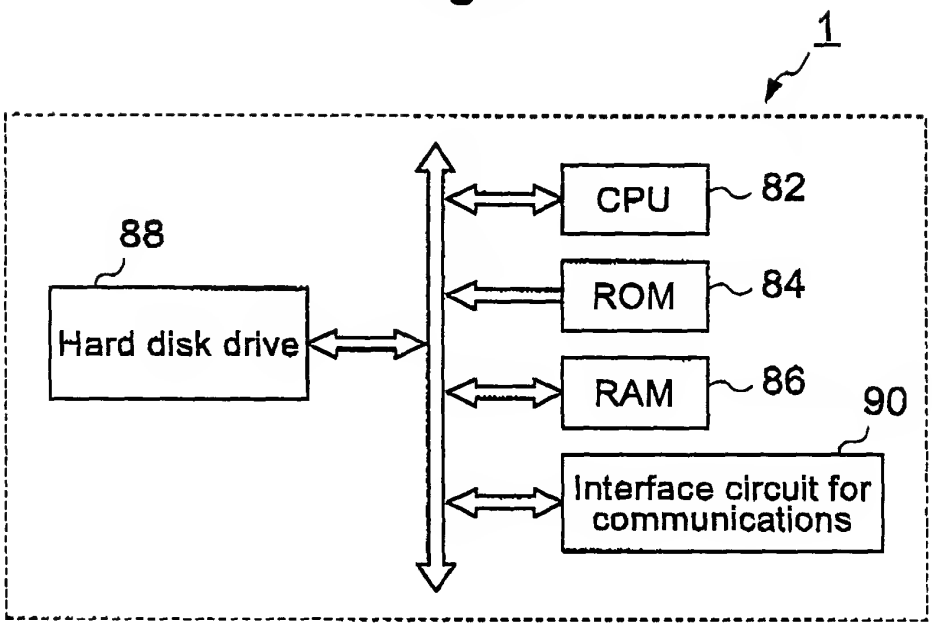

1
CPU
82
88
ROM
84
Hard disk drive
RAM
86
90
Interface circuit for communications

Fig. 6

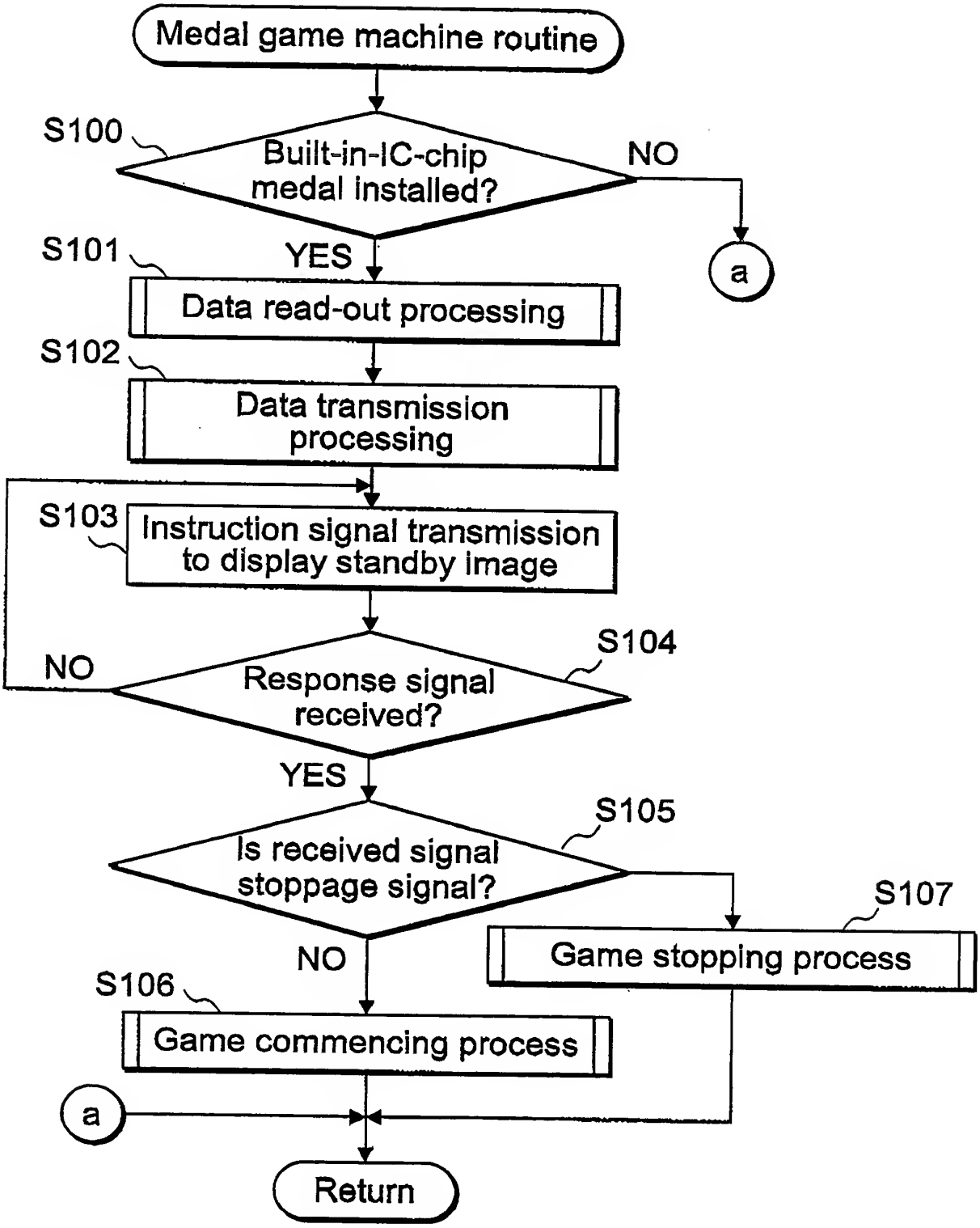
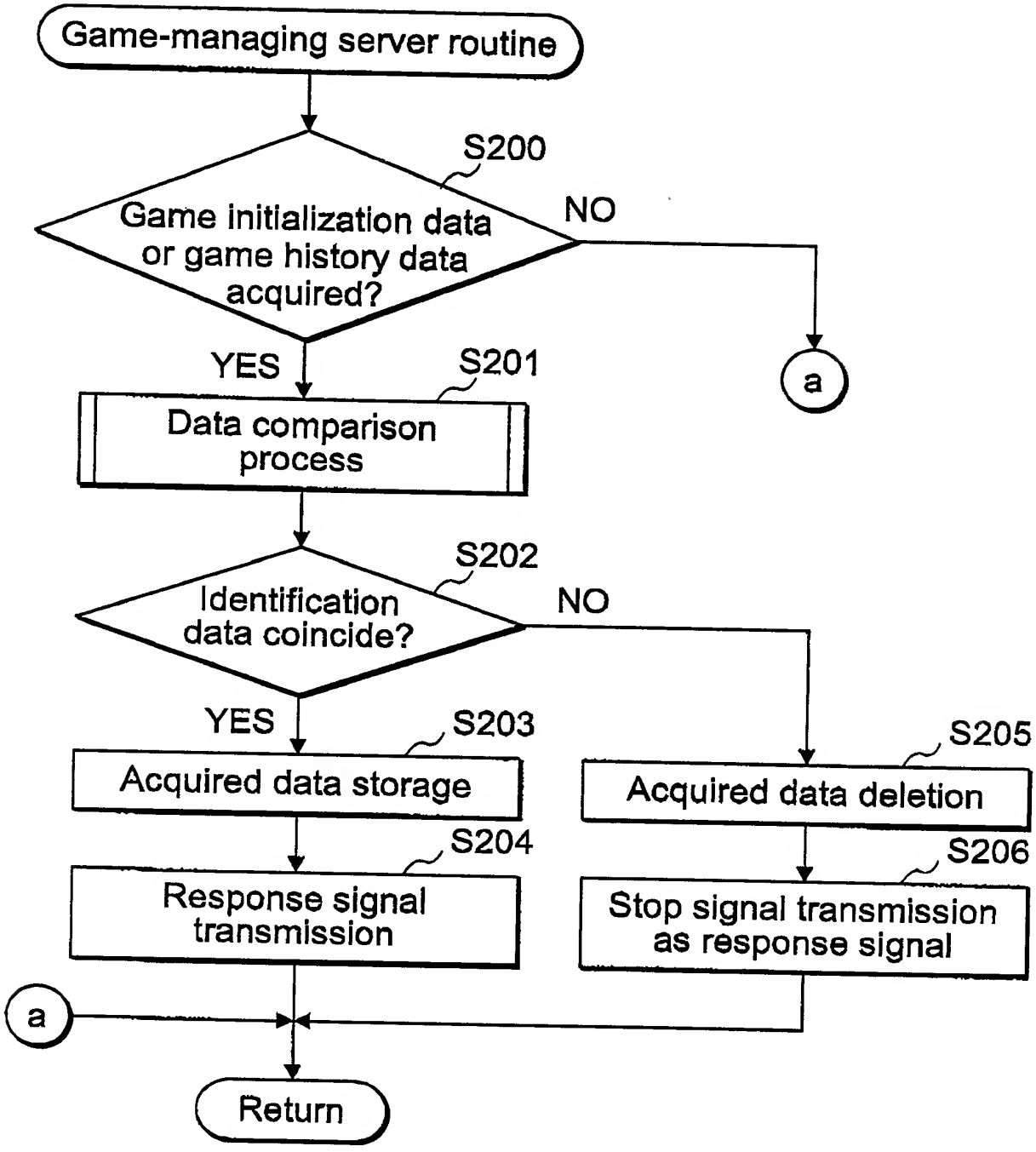

Medal game machine routine
S100
Built-in-IC-chip medal installed?
NO
YES
a
S101
Data read-out processing
S102
Data transmission processing
S103
Instruction signal transmission to display standby image
S104
Response signal received?
NO
YES
S105
Is received signal stoppage signal?
S107
Game stopping process
NO
S106
Game commencing process
a
Return

Fig. 7


Game-managing server routine
S200
Game initialization data or game history data acquired?
NO
YES
S201
Data comparison process
a
S202
Identification data coincide?
NO
YES
S203
Acquired data storage
S205
Acquired data deletion
S204
Response signal transmission
S206
Stop signal transmission as response signal
a
Return

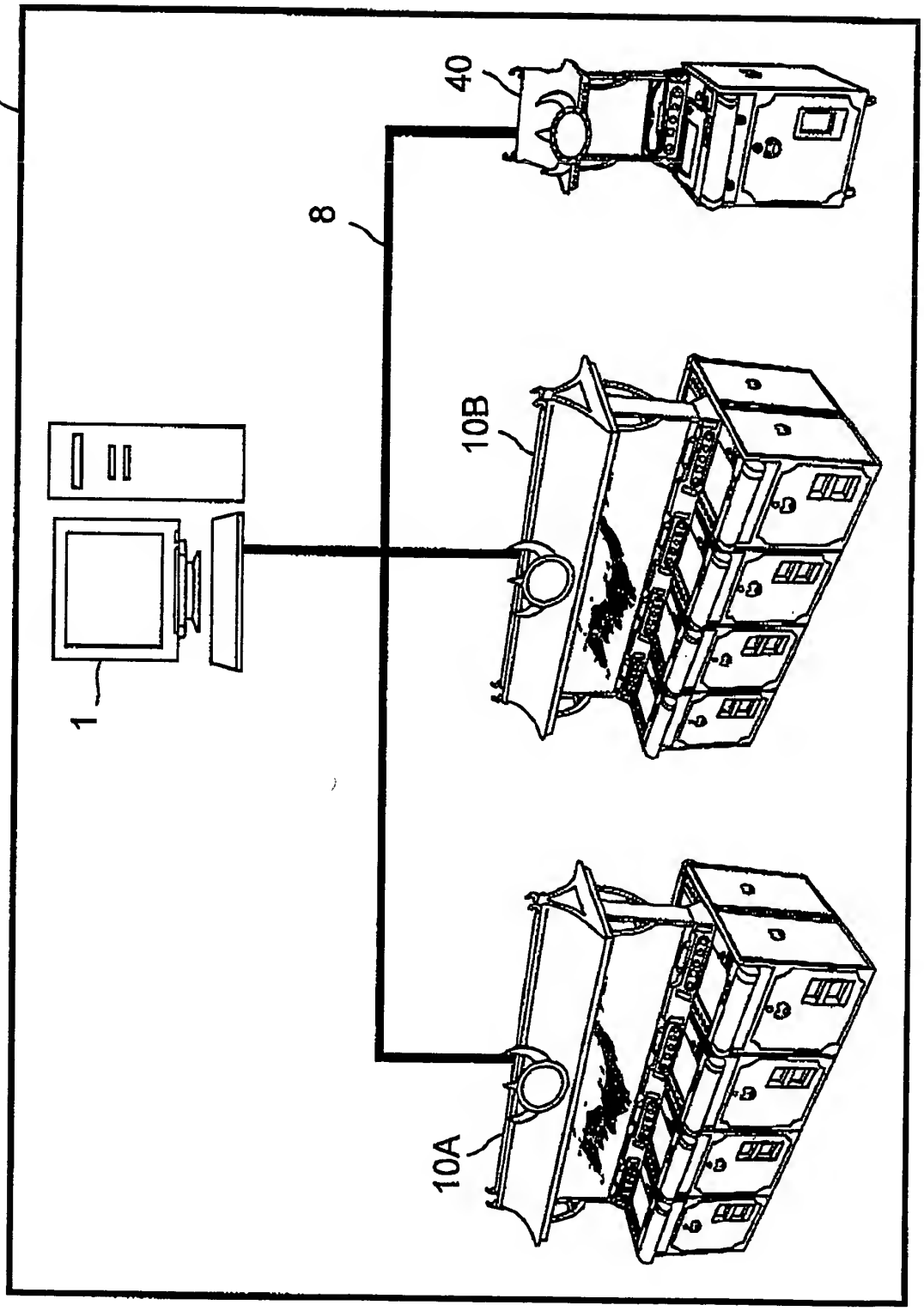



Fig. 8